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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **Kenji HOSHI et al.** Group Art Unit: **2814**

Serial No.: **10/073,314** Examiner: **Dana Farahani**

Filed: **February 13, 2002** Confirmation No.: **4466**

For: **SEMICONDUCTOR DEVICE AND ALIGNMENT SENSING METHOD FOR SEMICONDUCTOR DEVICE**

Attorney Docket Number: **020171**
Customer Number: **38834**

SUBMISSION OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

February 16, 2005

Sir:

Applicants submit herewith an Appeal Brief in the above-identified U.S. patent application.

Attached please find a check in the amount of $500.00 to cover the cost for the Appeal Brief.

If any additional fees are due in connection with this submission, please charge our Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANT

Ex parte **Kenji HOSHI et al.** (applicant)

SEMICONDUCTOR DEVICE AND ALIGNMENT SENSING METHOD FOR SEMICONDUCTOR DEVICE

Serial Number: **10/073,314**

Filed: **February 13, 2002**

Appeal No.:

Group Art Unit: **2814**

Examiner: **Dana Farahani**

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Date: **February 16, 2005**

BRIEF ON APPEAL

(I) REAL PARTY IN INTEREST

The real parties in interest are **FUJITSU LIMITED; KABUSHIKI KASHA TOSHIBA; and WINBOND ELECTRONICS CORP.**, by an assignment recorded in the U. S. Patent and Trademark Office on **May 21, 2002**, at Reel **012913**, Frame **0969**.

(II) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellant, appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(III) STATUS OF CLAIMS

Claims 1-4 and 13-16 are pending. Claims 1-4 and 13-16 stand rejected. No other claims are pending. No other claims have been allowed. The claims on appeal are 1-4 and 13-16.

(IV) STATUS OF AMENDMENTS

No Amendments have been filed subsequent to final rejection.

(V) SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer. As set forth in claim 1 and expanded on in claim 13 as presently presented, each of the alignment marks 14 comprises a micronized pattern of grooves 16. See page 8, line 17 to page 9, line 8 of the specification, as well as FIGS. 1A to 1C of the drawings. The micronized pattern with grooves 16 is designed to have a size smaller than a resolution limit of an alignment sensor which is utilized to align the wafer for processing. See page 13, lines 20 to page 14, line 5. See also FIG. 3 and page 11, line 14 to page 13 line 19 which

describes the relationship of the alignment sensor to the markers, 30. The micronized pattern has a pattern forming margin 64 larger than that of a device pattern 62 formed over the semiconductor wafer 60. See FIG. 2, and page 8, line 26 to page 9, line 8, as well as, page 10, line 25 to page 11, line 4. The relationship between the micronized pattern and the alignment sensor, as well as the pattern forming margin, results in an alignment marker which is superior to those of the prior art.

Independent claim 13 is also directed to a semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer. Similar to the embodiment encompassed by claim 1 above, each of the alignment marks 52 is divided by a micronized line-and-space pattern into a plurality of lines 56 extending along a first direction. In addition, each of the plural lines is divided into a broken line having a plurality of segments, 58 and 54. As shown in FIG. 6A, intervals 58 between the cavities 54 of one broken-line pattern 56 are offset from those 58 between the cavities 54 of an adjacent broken-line pattern 56. Thus, the alignment marks 52 are the line/space patterns of the first embodiment with the addition that they are two-dimensionally divided. See page 19, lines 20-25 of the specification.

Dependent claims 15 and 16 are directed to the micronized pattern having a pattern forming margin 64 larger than that of a device pattern 62 formed over the semiconductor wafer 60. See FIG. 2, and page 8, line 26 to page 9, line 8, as well as, page 10, line 25 to page 11, line 4.

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 13-14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,037,671 to ***Kepler et al.***

Claims 1-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,037,671 to ***Kepler et al.*** in view of Patent Application Publication (U.S. 2001/0019401) issued to ***Irie et al.***, and further in view of U.S. Patent No. 6,162,675 to ***Hwang et al.***

Claims 15 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,037,671 to ***Kepler et al.*** as applied to claim 13 above, in view of U.S. Patent No. 6,162,675 to ***Hwang et al.***

(VII) ARGUMENT

(a) Appellants' argument as to the rejection of Claims 13 and 14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,037,671 to *Kepler et al.*

Claims 13 and 14 are not anticipated by U.S. Patent No. 6,037,671 to ***Kepler et al.*** (hereinafter "***Kepler et al.***") because the reference fails to set forth a required element present in claim 13. Claim 14 is likewise not anticipated by nature of its dependency.

MPEP § 2131 sets forth the presently accepted standard for determining whether a reference anticipates the claims of an application within the meaning of 35 U.S.C. § 102. The MPEP quotes Federal Circuit decision, Verdegnal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 10501, 1053 (Fed. Cir 1987) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference e.g." and Federal Circuit decision Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989), "The identical invention must be shown in as complete detail as is contained in the .... claim." The Examiner is to apply this well known standard when evaluating a reference to determine if the examined claim reads thereon.

In the present instance, the Examiner has not properly construed the limitations of claim 13 which state:

> ... each of the alignment marks being divided by a micronized line-and-space pattern into a plurality of lines extending along a first direction, and
> each of the plural lines being divided into a broken line having a plurality of segments...

The Final Office Action issued September 21, 2004 responds to Applicants' earlier Amendment setting forth this limitation as a distinguishing feature from ***Kepler et al.*** Page 2, section 2 of the Office Action states:

> ...Kepler discloses in figure 3 alignment marks (the first one of the marks being the vertical lines at the most-top-right of the figure, and the immediate vertical lines below them; and the second alignment marks being vertical lines at the most-top-left of the figure, and the immediate vertical lines below them) in a line space pattern along a first direction (vertical); and each of the plural lines being divided into a broken line having a plurality of segments (that is the vertical segments of the above described alignment marks), as can be seen in the figure.

The Examiner does not cite to the text of ***Kepler et al.*** but only to the figure, which he gives the above interpretation to. However, the text of the ***Kepler et al.*** specification at column 4, lines 33-40 discloses:

> A set of global alignment marks is etched on main surface 21a, and comprises a plurality of first sections 22, each having an upper surface which is substantially flush or coplanar with main surface 21a, and a plurality second sections 23 separating first sections 22. Each second section 23 comprises a plurality of first trenches 23a spaced apart by first uprights 23b, each upright having an upper surface substantially flush with main surface 21a.

In other words, ***Kepler et al.*** is not disclosing "...alignment marks (the first one of the marks being the vertical lines at the most-top-right of the figure, and the immediate vertical lines below them; and the second alignment marks being vertical lines at the most-top-left of the figure, and the immediate vertical lines below them)..." as the Examiner states. In fact, the reference discloses a plurality of first sections 22 and second sections 23. These sections are not related so as to form a line as the Examiner submits. Rather, they are a set of global alignment marks which are positioned according to a stepper employed. See Col. 4, lines 41-43.

This is not a divulgence of the present invention which discloses and claims alignment marks 52 being divided by a micronized line-and-space pattern 56 into a plurality of lines extending along a first direction 56, and each of the plural lines 56 being divided into a broken line 54 having a plurality of segments 58. See FIG. 6A of the present invention's drawings. See page 19, lines 13- 24.

As cited above, Federal Circuit decision Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989), held "[t]he identical invention must be shown in as complete detail as is contained in the .... claim." As demonstrated above, **Kepler et al.** does

not disclose "the lines" as set forth in the present invention. Rather, the Examiner has set forth an overly broad interpretation of the reference which asserts that "lines" are present, where in fact there are none. For at least the foregoing reasons, the honorable Board is respectfully requested to reverse the rejection maintained by the Examiner.

(b) Appellant's argument as to the rejection of Claims 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,037,671 to *Kepler et al.* as applied to claim 13 above, in view of U.S. Patent No. 6,162,675 to *Hwang et al.*

Claims 15 and 16 are not obvious within the meaning of 35 U.S.C. §103(a) as being unpatentable over ***Kepler et al.*** (as applied to claim 13 above) by nature of their dependency. Hence, the preceeding argument applies to claims 13-16 equally. Further, the claims are not obvious because the reference relied upon by the Examiner does not teach the necessary limitation. The September 21, 2004 Office Action cites to ***Hwang et al.*** as disclosing in figure 15, a DRAM cell with a device pattern margin. The Office Action asserts that claims 15 and 16 would be obvious, because a change in size is generally recognized as being within the level of ordinary skill in the art. Claims 15 and 16 are both directed to the limitation of:

> ... a margin for forming the micronized pattern to be formed in is lager than a margin for a device pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

Appellants respectfully submit that ***Hwang et al.*** discloses neither pattern forming the margin of micronized pattern dividing the alignment mark larger than that of the device pattern, nor the relationship between pattern forming margins of micronized patterns. The feature offers a design of the alignment mark in which influences of the physical asymmetry of the alignment mark (WIS, Wafer Induced Shift) are reduced. Such a technical feature is not the result of a mere change in size within the level of ordinary skill. For at least the foregoing reasons, the honorable Board is respectfully requested to reverse the rejections maintained by the Examiner.

(c) Appellant's argument as to the rejection of Claims 1-4 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,037,671 to *Kepler et al.* in view of Patent Application Publication (U.S. 2001/0019401) issued to *Irie et al.*, and further in view of U.S. Patent No. 6,162,675 to *Hwang et al.*

Claims 1-4 are not obvious within the meaning of 35 U.S.C. §103(a) as being unpatentable over ***Kepler et al.*** (as applied to claim 13 above) in view of Patent Application Publication (U.S. 2001/0019401) issued to ***Irie et al.***, and further in view of U.S. Patent No. 6,162,675 to ***Hwang et al.*** because the references fail to set forth required elements present in claim 1. The references do not disclose the limitations as set forth by the Examiner.

The Final Office Action, September 21, 2004, page 3, section 3 states: "In regard to claim 1, Keplar discloses the limitations in the claims, as discussed above in regard to claim 13." In other words, the Examiner is applying the reference, as applied above, to the limitation of claim 1 which states: "...each of the alignment marks comprising a micronized pattern,..." Appellants refer to and incorporate herein the comments set forth in section (VII)(a) above. Appellants further submit as follows.

The present invention according to claim 1 has limitations relating to the micronized pattern 16 by which the alignment mark 14 is divided. First, the micronized pattern has a size smaller than a resolution limit of an alignment sensor (hereinafter "the first feature"), and (ii) the micronized pattern has a pattern forming margin larger than a device pattern formed over the semiconductor wafer has (hereinafter "the second feature").

The Examiner maintains that the first feature is an obvious matter based on the technical idea of the density filter disclosed in ***Irie et al.*** Specifically, the Examiner states:

> Irie discloses in figure 1 and at pages 4 and 5, paragraph [0066], that a density filter [of light] has light blocking portions, shaped as dots, wherein the size of the dots becomes less than the resolution limit of an optical system in which the density filter is used. Furthermore, Irie discloses this structure results in higher light attenuation rate.... Therefore, it would have been obvious to introduce the micronized pattern of the Kepler reference, such that it would have a smaller size than a resolution limit of an alignment sensor in order to increase the light attenuation rate. *(emphasis added)*
>
> -September 21, 2004, Office Action, page 3, section 3.

However, as disclosed in the response to two Office Actions, and as discussed during a telephone interview of June 4, 2004, Appellants submit that ***Irie et al.*** does not disclose the first feature of the present invention and the idea concerned with the density filter disclosed in ***Irie et al.*** is not equivalent to the first feature. The first feature offers a design of the alignment mark in which

influences of the optical asymmetry of the alignment sensor (TIS, Tool Induced Shift) are reduced. The consideration of the optical asymmetry of the alignment sensor is requisite for realizing the first feature. See page 15, lines 18-26 of the specification.

The Examiner maintains that this limitation would have been obvious in light of the teachings of ***Irie et al.*** Specifically, the teachings at paragraph [0066] and Figures 2A and 2B are referenced. As discussed in the interview of June 4, 2004 and set forth in the Amendment of June 23, 2004, paragraph [0066] does not disclose alignment marks on a semiconductor nor the micropattern forming the alignment marks being less than the resolution limit of an alignment sensor. Paragraph [0066] discloses dots on a density filter for the purpose of affecting a light attenuating rate. The density filter is not being utilized for alignment, and there is no disclosure of an alignment sensor such as to view the dots or to make an alignment mark from the disclosed dots. Hence, there is no basis for combining the teachings of ***Irie et al.*** with ***Kepler et al.***

Irie et al. only teaches that dots on a density filter may have a size below the resolution limits of an optical system for affecting the light attenuating rate to the end product (*i.e.*, substrate, 4). This teaching in combination with ***Kepler et al.*** does not result in the first feature (*i.e.*, the second element of claim 1).

In response to Appellants' repeated assertions of the above, the Examiner maintains in the September 21, 2004 Office Action:

> ...although the Irie reference is directed to light attenuation rate, the idea of the dots on a density filter correlating with the resolution limits of an optical system to affect the light attenuation rate is similar to the idea of the micronized pattern correlating with the resolution limit of the sensor, and this analogy of the two ideas is used to make the obviousness rejection. The structures of the two references are obviously different. *(emphasis added)*
>
> -page 5, section 5.

The Examiner submits on page 3 of the Office Action that light attenuation rate is a motivation for the combination of ***Keplar et al.*** and ***Irie et al.*** Then, the Examiner submits on page 5 of the very same Office Action that the motivation is not even one which ***Keplar et al.*** has any interest in accomplishing. The fact that **Irie et al**. may have similar ideas, and analogies may

be drawn, does not provide the necessary limitations, let alone provide the teaching, suggestion or incentive to make the combination with the other references.

The Examiner also regards the second feature as an obvious matter citing ***Hwang et al.*** Specifically, the September 21, 2004 Office Action states that a change in size is generally recognized as being within the level of the ordinary skill in the art. Appellants respectfully submit that ***Hwang et al.*** discloses neither pattern forming the margin of micronized pattern dividing the alignment mark larger than that of the device pattern, nor the relationship between pattern forming margins of micronized patterns. The second feature offers a design of the alignment mark in which influences of the physical asymmetry of the alignment mark (WIS, Wafer Induced Shift) are reduced. Such a technical feature is not the result of a mere change in size within the level of ordinary skill.

The combination of above-mentioned first and second features realizes a design of the alignment mark in which influences of both the optical asymmetry of the alignment sensor and the physical asymmetry of the alignment mark are reduced. The first and second features of the present invention are not reached without the inventors' assiduous consideration of the optical asymmetry of the alignment sensor and the physical asymmetry of the alignment mark. That is, these features are not simple technical matters easily achieved by the combination of ***Kepler et al.*** and ***Irie et al.*** or ***Hwang et al.***, because the first and second features are mutually related. For at least the foregoing reasons, the honorable Board is respectfully requested to reverse the rejection maintained by the Examiner.

In the event this paper is not timely filed, appellants hereby petition for an appropriate extension of time. The fee for any such extension may be charged to our Deposit Account No. 50-2866, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

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(VIII) CLAIM APPENDIX

1. (original): A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks comprising a micronized pattern,

the micronized pattern having a size smaller than a resolution limit of an alignment sensor, and

the micronized pattern having a pattern forming margin larger than that of a device pattern formed over the semiconductor wafer has.

2. (original): A semiconductor device according to claim 1, wherein

the micronized pattern is a line-and-space pattern.

3. (original): A semiconductor device according to claim 2, wherein

each of lines constituting the line-and-space pattern are divided into a broken line having a plurality of segments.

4. (original): A semiconductor device according to claim 3, wherein

positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

5-12. (canceled)

13. (original): A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks being divided by a micronized line-and-space pattern into a plurality of lines extending along a first direction, and

each of the plural lines being divided into a broken line having a plurality of segments.

14. (original): A semiconductor device according to claim 13, wherein

positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

15. (original): A semiconductor device according to claim 13, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

16. (original): A semiconductor device according to claim 14, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

(IX) EVIDENCE APPENDIX

No evidence under 37 C.F.R. § 41.37(c)(1)(ix) is submitted.

(X) RELATED PROCEEDING APPENDIX

No decisions under 37 C.F.R. § 41.37(c)(1)(x) are rendered.